INVERSION LAYER SOLAR CELL FABRICATION AND EVALUATION

Midway Report

DRD

by

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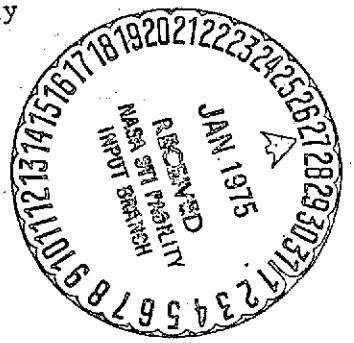

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ABSTRACT

Inversion layer solar cells have been fabricated by etching through the diffused layer on p-type silicon wafers in a comb-like contact pattern. The charge separation comes from an induced p-n junction at the surface. This inverted surface is caused by a layer of transparent material applied to the surface that either contains free positive ions or that creates donor states at the interface. Cells have increased from 3 ma I_{sc} to 100 ma by application of sodium silicate. The action is unstable, however, and decays with time.

SUMMARY

Transparent electrode cells that require a thin insulating coating of large area, with no leakage or shorts under bias, were extremely difficult to fabricate. Experiments designed to produce this layer were unsuccessful, yielding shorts or high leakage paths under bias. Substances such as silicon dioxide, silicon monoxide and sodium silicate were applied in various ways, and none yielded a defect-free transparent insulating layer.

The work on the transparent electrode cell was terminated and efforts directed to the development of a contaminated layer cell. The process developed seems to promise a cell which could be manufactured using state-of-the-art technology, and be adaptable to low cost large volume fabrication practices. An n-layer is first diffused on the silicon wafer surface; following diffusion of the n-layer, titanium-silver is then evaporated over the entire diffused surface. Using photolithography, a comb-like pattern is delineated exposing the titanium-silver. The titanium-silver is removed in the exposed areas by etching. With the photoresist still in place, the exposed diffused surface is then etched away exposing the base silicon. Mesas are thus formed. A coating of material designed to create donor surface states or supply positive ions on the surface is applied. Various substances were tried but the most successful was sodium silicate. A 2x2 mesa cell without an inversion region yields about 3 ma. After proper treatment with sodium silicate, outputs as high as 115 ma I_{SC} have been measured.

Other means of creating an inversion region such as sodium ions in silicon dioxide were not adequate.

Thus far, the sodium silicate layer has not produced a stable cell. After the sodium silicate is applied, the output decreases over a period of time to that of the cell before the sodium silicate was applied. The prime endeavor will be to obtain a stable coating.

I. INTRODUCTION

A. Basic Conventional Cell Description

In a conventional diffused p-n junction, solar cell power is extracted from the cell by the separation of light generated hole electron pairs within the built-in electric field across the junction. This field results from the diffusion of p-type carriers (holes) from the p-type bulk into the n-type area and the diffusion of n-type carriers (electrons) into the p-type bulk.

The collection efficiency of a solar cell is the probability that a hole electron pair will be separated in the electric field before recombination takes place. The collection efficiency depends on how far away from the junction hole electron pair generation takes place and on the diffusion length of the generated carriers.

For maximum efficiency certain trade-offs must occur. A thick n region is desirable to obtain a low series resistance. However, a thick n layer means that hole electron pairs generated close to the surface by shorter wavelengths of light must travel a longer distance to reach the junction. This increases the probability that they will recombine before reaching the junction. The optimum junction depths must be selected from a compromise between these two criteria.

Another area where a trade-off occurs is in the doping level of the n diffusion. A high doping level is desired to obtain a low series resistance. However, a high doping level results in a short recombination time which will decrease the collection efficiency of the cell for shorter wavelengths of light.

The end result of these trade-offs is that efficiency in the short wavelengths of light is sacrificed in order to improve the overall performance of the cell.

B. Basic Transparent Electrode Cell Description

It is proposed that a solar cell with a thin induced inversion region would be more efficient in the shorter wavelengths of light than a standard diffused cell. This inversion region would occur right at the surface of the cell which would reduce the distance that hole electron pairs generated by short wavelengths of light would have to travel before being collected.

One method of inducing an inversion region is to use the capacitor principle to attract electrons to the surface from the bulk of a p-type wafer and to repel positive carriers away from the surface of a p-type wafer. This creates an inversion region next to the surface of the wafer. This principle is used in the transparent electrode cell whose cross section is shown in Fig. 1. The transparent electrode must be biased positively with respect to the back contact of the cell in order to induce an n region at the surface of the wafer. An electric field is formed across this inversion region similar to the electric field across the junction in a diffused solar cell. This electric field can be used to separate light generated hole electron pairs. The n diffusions shown in Fig. 1 are there to make contact with the inversion region.

An inversion region can also be induced in a p-type wafer by fixed positive ions in a transparent layer on the wafer surface.

The contaminated oxide cell uses sodium ions incorporated into a thermally grown silicon dioxide layer. The ions are introduced into the

silicon dioxide by mixing NaCl with the water that is boiled and passed through the furnace where oxidation takes place.

II. TRANSPARENT ELECTRODE CELL

A. Transparent Electrode Growth

The problems of growing a consistent transparent electrode have been solved by modifying the transparent electrode growth apparatus. The new setup is pictured in Fig. 3. It is believed that much of the SnO_2 was deposited on the sides of the long furnace tube in the old apparatus, rather than on the wafer. In the new apparatus the wafer is placed on a ceramic heating block and placed in a 10" long tube. The wafer is heated by passing a current through the tungsten wire incorporated in the heating block. The normal mixture of $SnCl_3$ fumes, nitrogen, and oxygen is then passed through the tube. This method produces more consistent results than the old method.

B. Low Temperature Insulating Oxides

In order to reduce the time and complexity involved in processing transparent electrode cells, much work was done in the area of growing low temperature oxides. Growth of oxides at relatively low temperatures increases cell efficiency in that a high temperature oxidation will cause lattice faults which reduce the recombination time for hole electron pairs. In addition, a low temperature oxide will not drive the n-diffusion deep into the wafer.

C. Methods of Testing Dielectrics

In order to test the dielectric integrity of the various oxides that were tried, a pattern of conducting dots was put on the oxide to be checked. A square array of eight dots on a side was used. Conducting silver

paint was used to form the dots. The breakdown characteristic of the oxide was then tested on a Type 575 curve tracer. Contact was made to the back surface of the cell by a brass block and a movable needle point was used to make contact to each dot in turn. Since the dots covered approximately 50% of the total cell area, a good estimate of the number of dielectric faults per unit area could be obtained. A diagram of this test apparatus is shown in Fig. 4.

In previous work with the transparent electrode subcells, it was found that a 3000 Å insulator was optimum. Using this oxide thickness, it was found that a positive bias with respect to the back contact of 50 v was sufficient to create a strong inversion layer. Therefore, all dielectrics fabricated were tested for breakdown at an applied voltage of up to 50 v.

Another method was tried to test breakdown voltages of the different dieletric. After the dielectric coating had been applied, the wafer was placed in transparent electrode growth apparatus with a steel washer on top of the wafer. It was thought that the steel washer would prevent the SnO_2 from forming around the periphery of the wafer, leaving a circle of the transparent electrode material in the center of the wafer. This did not work as expected, however, because the SnO_2 would also form underneath the steel washer which resulted in the transparent electrode shorting to the edges of the wafer. Since it would take a significantly longer time to etch the transparent electrode away from the edges than it would be to paint on the matrix of silver dots, the silver dot method was used to test dielectric breakdowns.

D. Growth of SiO_2 Using $SiCl_4$

The first dielectric to be tried was SiO_2 grown at low temperature by a reacton of silicon tetrachloride and oxygen on the surface of the wafer.

The apparatus used to grow the SiO_2 is shown in Fig. 5. Nitrogen is used as an inert medium to carry the $SiCl_4$ fumes into the reaction chamber where the $SiCl_4$ combines with the oxygen to form SiO_2.

Experiments were made using a wide range of temperatures and flow-rates in an effort to produce a faultless oxide layer. It was found that the flowrates of the nitrogen and oxygen had little affect on the oxide produced, or on the rate at which the oxide grew. Temperature was found to be the critical factor, and temperatures from 0°C to 300°C were tried. It was found that a temperature of 0°C produced the best SiO_2 layer using this method.

After applying the silver dots and testing, it was found that none of the areas tested would stand up to the 50v bias. The reason for this was evident after examining the oxide layer with a microscope. There were many pinholes and imperfections which would allow shorts to occur.

Next a commercially available spin-on oxide was tried. The spin-on oxide selected was Emulsitone's Silicafilm SiO_2. The oxide was spun on at 5000 rpm which resulted in an oxide thickness of approximately 3000 Å. After spinning, the wafer was heated to 300°C for 5 minutes to harden the oxide layer.

Testing the oxide using the silver dot method showed that most of the cell area would not support a bias of 50v. Only about 10% of the area withstood the full 50v bias.

Again examination under a microscope showed that many pinholes and faults existed in the oxide layer. The pinholes were not as numerous or as large as those that occurred using the $SiCl_4$ and oxygen reaction method, however.

It was thought that spinning several thin layers whose thickness added up to 3000 Å would help alleviate the pinhole problem. If pinholes were a purely random occurrence, the probability of having a pinhole in an identical position through several layers of oxide would be small.

Again testing showed that only 10% of the cell area would withstand the 50v bias. Evidently once a pinhole is formed in the initial oxide layer, the defect will propagate through successive layers of oxide that are spun on at a later time. The exact cause of the pinhole problem is not clearly understood. It could be that there are extremely small particles in the spin-on oxide solution that cause pinholes. In addition, some sort of surface contamination could occur on the wafer even though the wafers were cleaned thoroughly before processing.

A spin-on SiO_2 made from methanol, deionized water, and silicon tetrachloride was tried. After the spin-on solution was mixed, it was thoroughly filtered in an effort to remove all particulate contamination. A single coat of SiO_2 was spun on at 5000 rpm and baked for 5 minutes at 300°C.

Again testing showed that only about 10% of the cell area would not break down under a 50v bias. Spinning several coats of the SiO_2 mixture on the wafer did not improve the 10% figure appreciably. The results obtained with the mixure of methanol, deionized water, and silicon tetrachloride produced the same results as had been obtained with the commercial spin-on.

E. Slow Evaporation of SiO

An evaporated coating of SiO was tested next. The SiO was evaporated at a slow rate in a vacuum of 10^{-5} Torr. It was thought that a slow evaporation rate might promote the formation of SiO_2 on the wafer surface through combination of the SiO and the residual oxygen in the vacuum chamber. It was

desired to form SiO_2 on the wafer rather than SiO due to the fact that SiO_2 has a higher dielectric breakdown.

Testing showed that approximately 60% of the cell area would not break down under a bias of 50v. Close inspection under a microscope did not reveal any pinholes. There could be small pinholes in the oxide that could not be resolved by the microscope, however. The evaporation of several thin coats of oxide to make up a 3000 Å dielectric did not improve the results. Again only about 60% of the cell area would take a 50v bias.

F. Sodium Silicate Insulating Layers

The dielectric that produced the best results was a spin-on solution of sodium silicate diluted with deionized water. A solution of two parts deionized water to one part sodium silicate was mixed and thoroughly filtered to remove any particulate matter. The sodium silicate was spun on the wafer at 500 rpm and baked for 5 minutes at 300°C.

It was found that 90% of the cell area would support a bias of 50v. Approximately half of the faults located were not shorted initially. These faults would appear at some period of time ranging from 5 minutes to 1 hour after the 50v bias was applied. It was also noted that some of the faults could be "burned out" by briefly applying a high voltage to the silver dot where the fault was located. Unfortunately, not all of the short-circuited areas could be repaired this way.

G. Discussion of Perfection of Insulating Layers

None of the low temperature dielectrics fabricated would be suitable for a full 2x2 cm transparent electrode solar cell. Many wafers were fabricated using the different dielectrics and not one was entirely free of dielectric breakdowns at a bias of 50v.

In order to obtain a comparison between the dielectric strength of the low temperature dielectrics and a high temperature steam grown oxide, the silver dot pattern was applied to a wafer with a 3000 Å steam grown oxide. Every silver dot in the 8x8 matrix withstood a 50v bias. The bias had to be increased to nearly 100v before breakdown occurred.

The fact that no breakdowns occurred was not consistent with results obtained in fabricating the transparent electrode subcells. It was found when testing the subcells that approximately 20% of the subcells on each wafer exhibited some form of breakdown before a bias of 50v was reached.

The 20% failure for the subcells can be explained by the fact the HF etch faults exist in thermally grown SiO_2 layers. The HF penetrates into and removes the SiO_2 in the faults very quickly. This leaves an opening where the transparent electrode material can short to the p-type surface of the wafer very easily. These electrical short circuits caused by etch faults make processing a full 2x2 cm transparent electrode cell even with a thermally grown oxide nearly impossible.

H. Spin-on Transparent Electrodes

A commercially available spin-on transparent electrode material was evaluated to find out whether or not it could be etched successfully without the use of HF. The material used was Emulsitone Solution #673. After the wafer had a 3000 Å thermal oxide grown on the surface, the spin-on transparent electrode was spun on and baked. A photoresist pattern was applied over the transparent electrode. A paste made of powdered zinc and Karo syrup was painted over the surface of the wafer and the wafer was placed in a solution of one part deionized water to one part HCl. This procedure removed most of the transparent electrode material from the areas to be etched. Successive

etches did not remove any more of the undesired transparent electrode. HF removed the remaining transparent electrode material, however, but the use of HF resulted in the occurrence of short circuits from the transparent electrode to the p-type silicon wafer.

At this point it was decided to abandon efforts to produce a large area transparent electrode cell. The problems associated with fabricating a perfect dielectric and etching of the SiO_2 layer cannot be solved with current processing techniques. Work was then started on the Mesa cell as described in the following section.

III. MESA CELL

A. General Description

The Mesa Cell as pictured in Fig. 2 is constructed by diffusing an n-type dopant into a 2x2 cm p-type wafer. A forty-minute diffusion was done at 945°C using a $POCl_3$ source. Then the metal contact was evaporated over the front surface of the wafer. Photoresist was applied and developed into the contact pattern. The metal was then etched from the areas not protected by photoresist. A silicon etch was used to remove the n diffusion from all areas not covered by the metal contact pattern. Metal was evaporated over the back surface of the wafer and the wafer was sintered. A solution of NaCl and sodium silicate was then spun on the front surface of the wafer.

The operation of the Mesa Cell is probably due to one of two possible causes. One is the same as the Contaminated Oxide Cell that was constructed and reported previously, and the other is the surface state cell reported previously, also. In the contaminated oxide cell a proportion of the sodium atoms in the sodium silicate layer are ionized. These positive ions repel positive carriers at the silicon surface and attract negative

carriers to the surface. This creates a narrow inversion region very close to the silicon-sodium silicate interface. The electric field within this inversion region can be used to separate light generated hole electron pairs in the same manner that electron hole pairs are separated in a conventional diffused p-n junction solar cell. In the surface state cell, donor states created by the sodium silicate layer create an inversion layer because of the layer of free electrons from the surface states in the p wafer at the surface. An electric field and an induced p-n junction is thus formed.

The primary advantage of the Mesa Cell is the short amount of time required to process cells. Two high temperature oxidation steps and a low temperature diffusion were needed to fabricate contaminated oxide cells. A single low temperature diffusion is all that is required in the processing of a Mesa Cell. The lack of exposure to high temperatures (1100°C or above) will tend to increase the efficiency of the Mesa Cell. Exposure of single crystal silicon to a thermal cycle from room temperature to 1100°C or more and then back to room temperature creates lattice faults which tend to reduce the recombination time which will lead to an overall decrease in efficiency of a solar cell.

Three photoresist steps are required in the processing of a contaminated oxide cell, one to open holes in the initial oxide to allow diffusion to occur, one to open contact areas in the contaminated oxide, and one to etch the metal contact pattern. Only one photoresist operation to etch the metal pattern is required to fabricate the Mesa Cell. The simplified process schedule also increases the yield for a given batch of cells.

The procedure of diffusing the entire surface of the Mesa Cell eliminates many of the leaky junctions that occurred in the processing of

Contaminated Oxide Cells, due to high leakage from contact to the p wafer. When doping the photoresist process in fabricating Contaminated Oxide Cells, either defects in the mask or impurities in the photoresist, would cause spots of photoresist to remain over areas that should be etched off for diffusion to occur. This would result in electrical short circuits across the junction due to the metal contacts making electrical connection to the p-type bulk.

B. Mesa Cells with Aluminum Contacts

The first successful Mesa Cells had a junction depth of 3-4μ which resulted from a 40 minute $POCl_3$ diffusion at 945°C. The silicon was etched to a depth of approximately 7μ. A solution of 5 ml of HF to 45 ml of nitric acid was used to etch the silicon.

Aluminum was used as the contact metal because of its resistance to the silicon etchant. Even if the protective photoresist peels off the aluminum contact pattern during the silicon etch, the aluminum will not be entirely etched off during the remainder of the etch. A detailed process schedule for the Mesa Cell is given in the Appendix.

The sodium silicate, used as the contaminated spin-on source, was made from a solution of two parts deionized water to one part sodium silicate with 1% by weight of NaCl added. It was found that this sodium silicate layer formed a good antireflection coating. The spin-on sodium silicate layer is also transparent to short wavelength light.

The V-I curve for the first successful Mesa Cell is shown in Fig. 6. Immediately after the sodium-silicate spin-on and a 5 minute heat treatment at 250°F, the cell output was raised from 5 ma to 90 ma short circuit current; the open circuit voltage was 0.54 volts. The efficiency of this cell is 3.2%. The low efficiency and poor curve factor of this cell is due to several

reasons, among them are the following: Aluminum is not the optimum contact material due to a significant series resistance between the aluminum and the silicon. The induced inversion is very thin which will also produce a high series resistance. And, a contact pattern with thirty or forty fingers rather than the twenty finger pattern used on this cell, should decrease the series resistance caused by the thin inversion region.

It was noted that over a period of several days the output of the cell dropped from 90 ma to 75 ma. The lower value of short circuit current indicates that the inversion region had diminished. A five minute heat treatment at 250°F brought the short circuit back up to 90 ma. It is thought that the degradation in output over a period of time could be due to the humidity in the atmosphere penetrating the sodium silicate layer and through some mechanism passivating the contaminated layer. Perhaps a coating of some material that is transparent yet will serve as a moisture barrier applied to the Mesa Cell immediately after heat treatment would prevent this decrease in output.

C. Mesa Cell with Titanium-Silver Contacts

The next group of Mesa Cells that were processed had titanium-silver contacts. Titanium-silver contacts were used in an effort to reduce the series resistance of the cell. Much difficulty was encountered in doing the silicon etch after the titanium-silver contact pattern had been etched. The silicon etchant would undercut the titanium-silver very quickly causing the photoresist to lift around the periphery of the contact pattern resulting in severe contact damage.

The output of cells constructed using a shorter silicon etch time would not increase appreciably after spinning on sodium silicate, and heat treating. This was thought to be caused by the stained area around the

periphery of the contact pattern where the silicon etch had attacked the titanium-silver. This stained area could be insulating the inversion layer from the n diffusion.

D. Wax Etch Masks

In order to overcome the problem of undercutting that occurred when photoresist was used as a mask against the silicon etch, a method of using Apiezon wax as a mask against the silicon etch was devised. A set of twenty razor blades with spacers between the blades was used as a stencil to apply the wax. The wafer to be etched was heated to a temperature slightly greater than that required to melt the wax. The razor blades were dipped in molten wax and pressed down on top of the wafer. This left a set of twenty parallel lines of wax on the wafer. The broad center contact was put on with a thicker blade using the same method. The wax pattern solved the undercutting problem and it was possible to do a deep etch (7μ) without seriously undercutting the titanium-silver contact.

Again, after spinning on sodium silicate and giving the wafers a five minute heat treatment, the outputs did not come up appreciably. The outputs ranged from 5 ma to 7 ma. Close inspection of the wafers under the microscope again revealed a stained area around the periphery of the contact area. As before, this was thought to be the reason for the poor output obtained.

The titanium-silver contacts did improve the series resistance of the cell. A resistance of .5 Ω was obtained with titanium-silver versus the .8 Ω series resistance obtained when aluminum contacts were used.

E. Buffered Silicon Etch

At this point a number of experiments were performed to develop a milder silicon etch that would be compatible with the photoresist process and that would not cause staining. It was found that a silicon etch consisting of, by weight, 8% hydrofluoric acid, 32% nitric acid, and 60% acetic acid met the preceding criteria. In order to prevent staining from occurring, the beaker containing the silicon etchant and the wafer undergoing the etching process had to be quenched with large amounts of deionized water when the etch was terminated.

A group of cells was fabricated using the new silicon etch solution. Prior to spinning on sodium silicate, the cells were examined under a microscope. There was no appreciable staining evident around the contact fingers. Again, after spinning sodium silicate and heat treating the wafers for 5 minutes at 250°F, the outputs remained low.

F. Low to High Output

After a period of approximately two weeks, all Mesa Cells previously fabricated were retested using a different heat treatment. The heat treatment started out at 250°F and progressed to 700°F in 50°F increments.

A V-I curve for a typical Mesa Cell with aluminum contacts is shown in Fig. 7. The short circuit current is 92 ma and the open circuit voltage is .46v after a heat treatment of 5 minutes at 250°F. After a heat treatment of 5 minutes at 400°F, the short circuit remains at 92 and the open circuit voltage increased to .5v. After a further heat treatment of 5 minutes at 600°F, the short circuit current increased to 96 ma and the open circuit voltage increased to .52 volts. The efficiency of this cell increased from 2.9% to 4.4% after heat treatment. The V-I curves for this cell after the

400°F heat treatment and the 600°F heat treatment are shown in Fig. 8 and Fig. 9.

A V-I curve for a Mesa Cell using titanium-silver contacts with the razor blade pattern is shown in Fig. 11. The short circuit current is 100 ma and the open circuit voltage is .52v. An efficiency of 4.9% is obtained with this cell. Initially, the output on this cell was low. After a period of several weeks, the cell was given a further heat treatment to 700°F which produced the results given.

A V-I curve for a Mesa Cell with titanium-silver contacts that was etched using the photoresist process is shown in Fig. 12. The short circuit current is 110 ma and the open circuit voltage is .49v. This cell was given a heat treatment up to 700°F and the output still remained low (around 6 ma). The cell was given the same heat treatment several weeks later which produced the results given. The overall efficiency of this cell is 4.3%.

G. Degradation of Cell Output

All cells whether constructed with aluminum or titanium silver contacts will degrade over a period of time. Typically, a cell output will drop by 20% of its peak in 24 hours. Over a period of weeks the cells will decrease in output back to the initial value obtained before the contaminated layer was spun on. This degradation is thought to be due to humidity penetrating the sodium silicate layer.

It is not understood why cells with aluminum contacts and a deep silicon etch will increase in output immediately after the sodium silicate is spun on and heat treated whereas it takes a period of weeks before the titanium silver cells with a relatively shallow etch to respond to the sodium silicate spin and heat treatment.

A cell that had shown an increased output after several weeks had the sodium silicate removed in diluted HF solution. Testing showed that the cell output had dropped down to the 6 ma measured prior to spinning on the sodium silicate. Another layer of sodium silicate was spun on the cell and given a heat treatment of 700°F. The output immediately returned to 90 ma. This indicates that some change must take place at the surface of the silicon wafer in order for the output due to the inversion region to increase.

IV. MEASURING APPARATUS

The apparatus used to trace V-I curves of the solar cells tested is pictured in Fig. 10. A variable resistor is used to load the cell in order to obtain the V-I curve. When the variable resistor is set to zero ohms, the short circuit current is obtained. When the variable resistor approaches infinite ohms, the open circuit voltage is obtained Either the sun or a Sylvania FBE lamp can be used as a light source for the curve tracing setup.

The breakdown tests were made with the circuit shown in Fig. 4. A Type 575 curve tracer was used to supply the sweep voltage and to display the magnitude of the breakdown.

V. CONCLUSIONS

Producing a transparent electrode cell of large area with any yield is very difficult. The main problem is applying a thin transparent insulating layer that is free from leakage paths through it. Therefore, a bias voltage strong enough to cause inversion could not be maintained and subsequently no cells were produced.

The contaminated oxide cell can be fabricated, however, and full attention was directed toward it. The mesa type inversion cell with a contaminated layer was initiated and cells fabricated.

Sodium silicate has been the only substance to produce an adequate conversion. Unfortunately, this substance is deliquescent and a deterioration of the cell characteristics with time occurs.

Since some cells are increased from 3 ma to 100 ma I_{sc} upon application of a reactive layer and return to 3 ma when the layer is removed, leads to the conclusion that there is a creation of an induced p-n junction at the surface of the cell. Because the U.V. response is increased, an inversion layer probably lies close to the surface.

VI. FUTURE INVESTIGATION

Effort will be expended to investigate different materials to find one that creates a strong inversion with stability. New silicon etching solutions will be tried to slow down the etching time and thus control the mesa depth better. Encapsulation will be considered to prevent the deterioration of the cells made with sodium silicate. Other means of creating a contaminated oxide such as a spin-on silicon dioxide contaminated with a sodium compound will be investigated.

APPENDIX

FABRICATION PROCEDURE FOR MESA CELL

1. Clean wafer by scrubbing with acetone and isopropyl alcohol.
2. Rinse to 2MΩ in deionized water.
3. Diffuse in a $POCl_3$ atmosphere for 40 minute at 945°C.
4. Dip wafer in HF for 10 seconds.
5. Rinse to 2MΩ.
6. Evaporate contact metal over front surface.
7. Apply and develop contact pattern photoresist.
8. Etch metal.
9. Do a silicon etch for desired length of time.
10. Evaporate metal on back of cell.
11. Sinter cell for 2 minutes at 600°C in a reducing atmosphere.
12. Spin on sodium silicate solution for 20 seconds at 5000 rpm.
13. Give cell desired heat treatment.

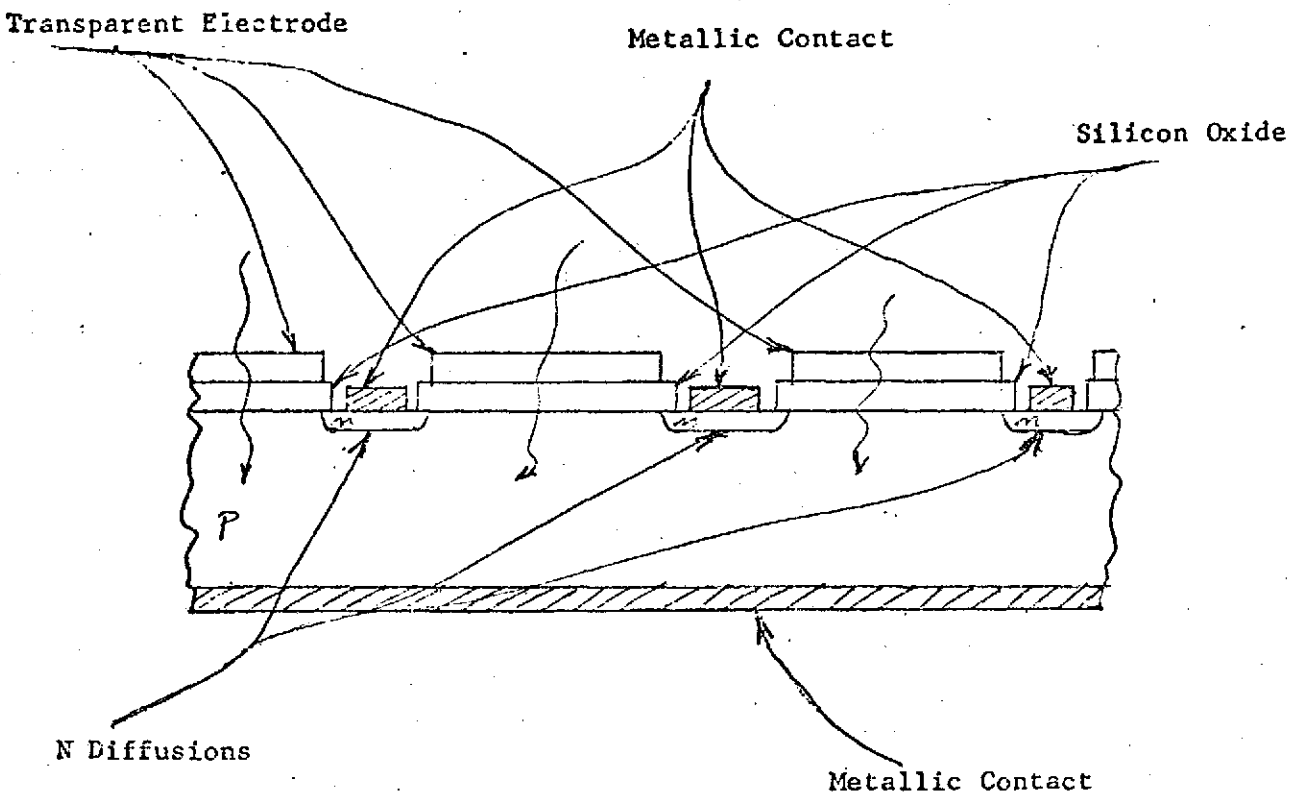


Figure 1

Transparent Electrode Cell

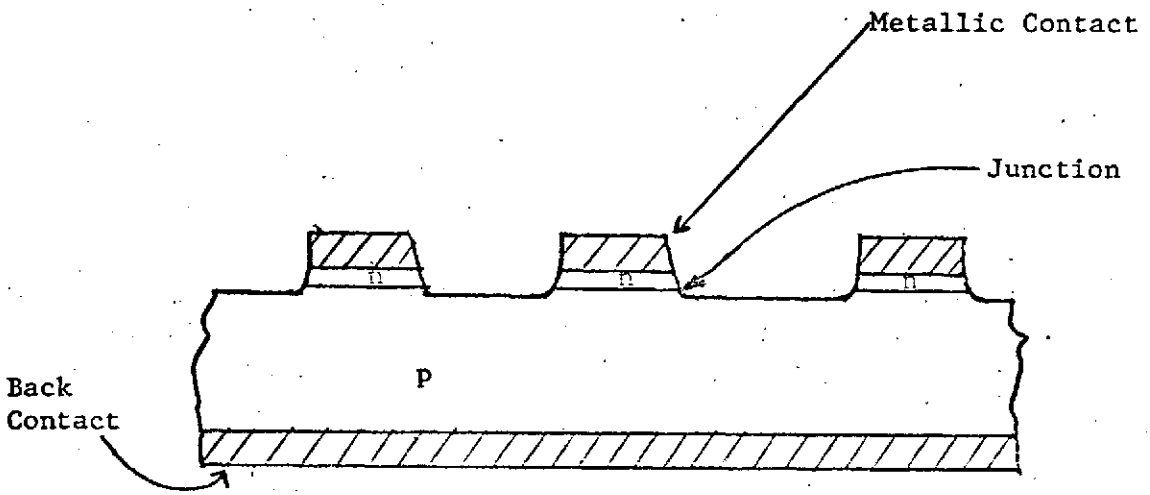


Fig. 2 Mesa Cell Without Positive Charged Layer and Inversion Layer

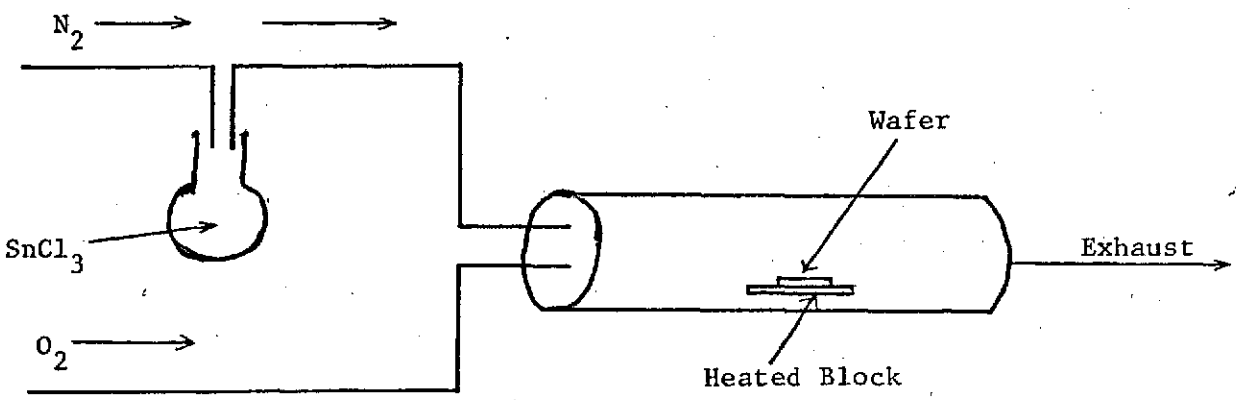


Figure 3 New Transparent Electrode Growth Apparatus

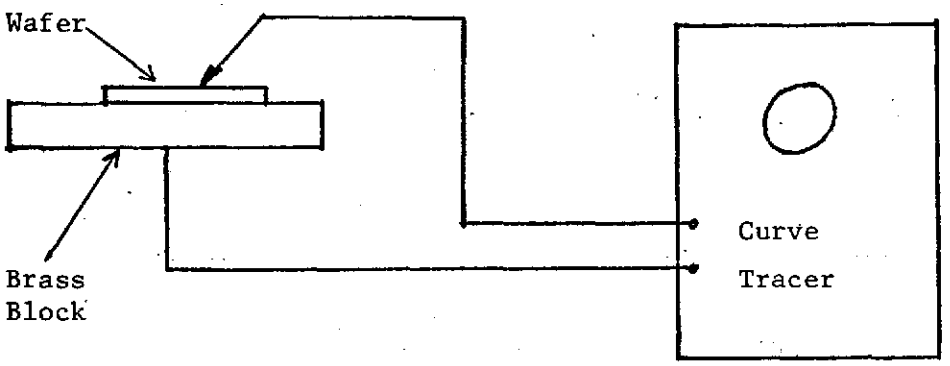


Figure 4 Breakdown Voltage Test Apparatus

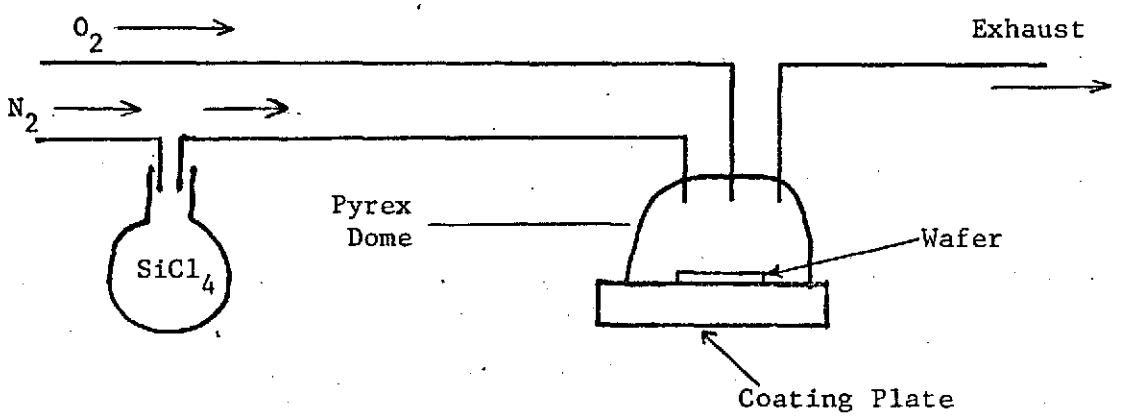


Figure 5 Apparatus to Grow SiO_2 Using $SiCl_4$

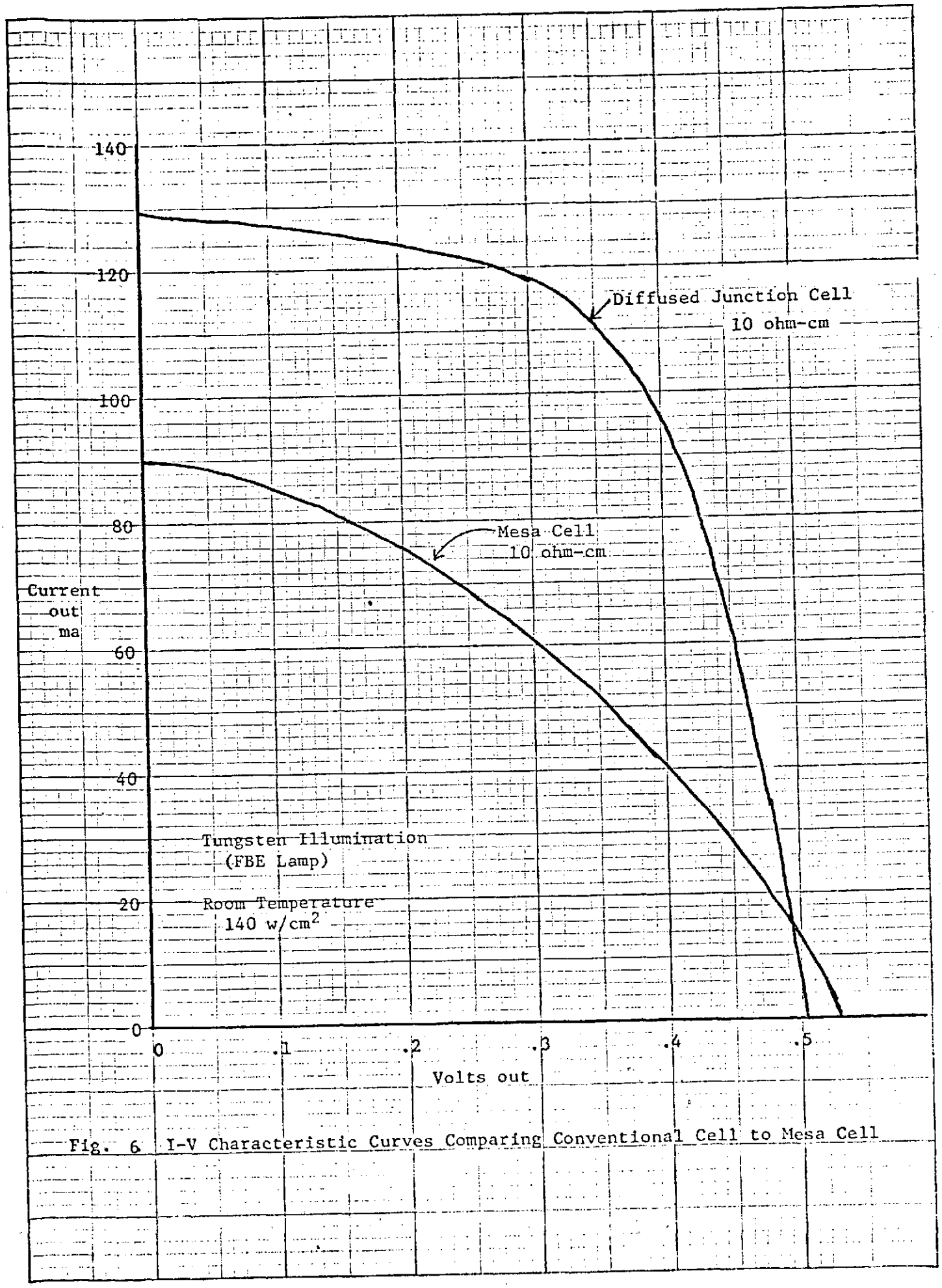


Fig. 6 I-V Characteristic Curves Comparing Conventional Cell to Mesa Cell

Figure 7

Inversion Layer "Mesa" Cell
Artificial Light
140 mw/cm^2 intensity
Room Temperature
Sodium Silicate Layer heated to
250°F for 5 minutes

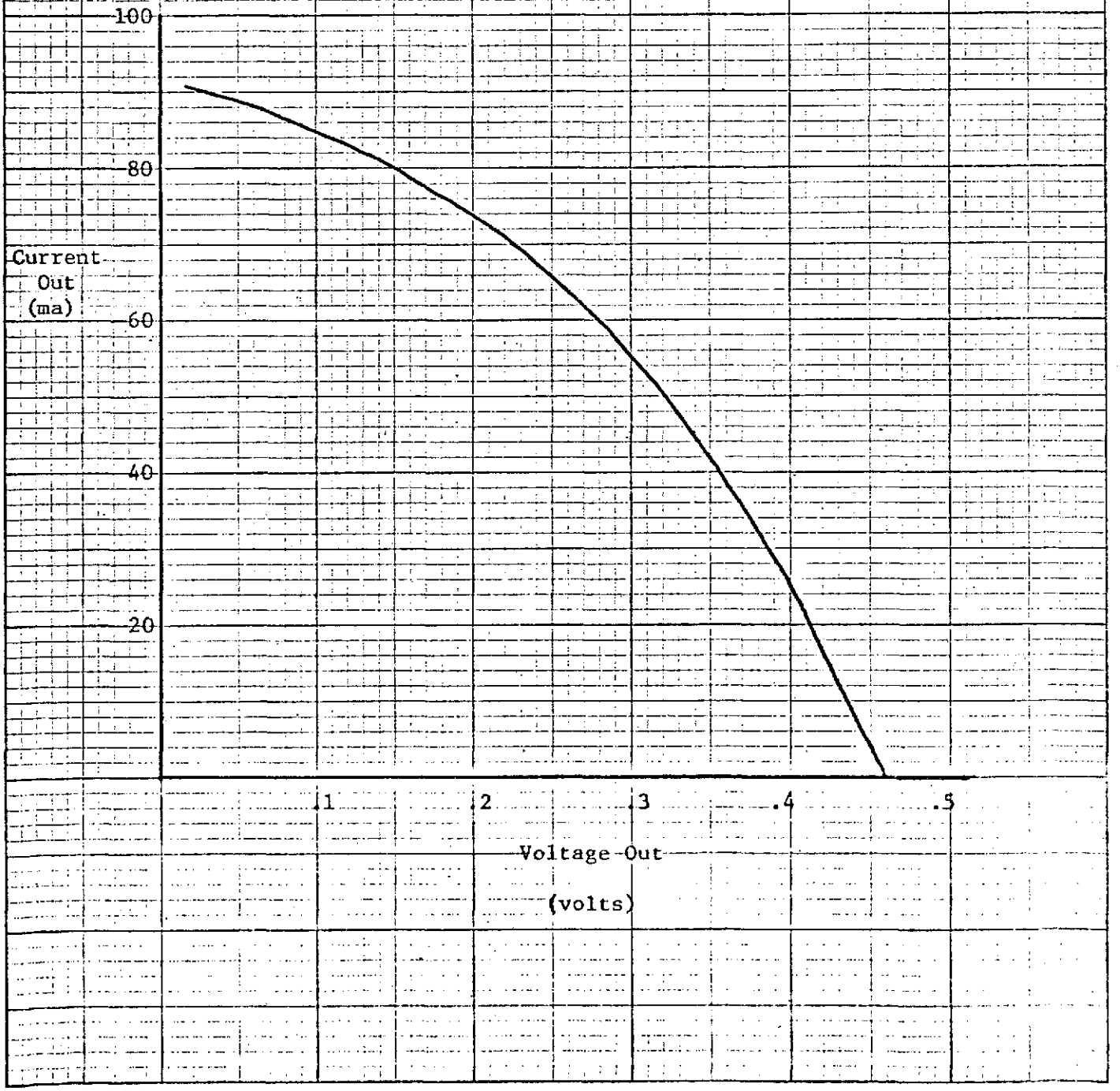
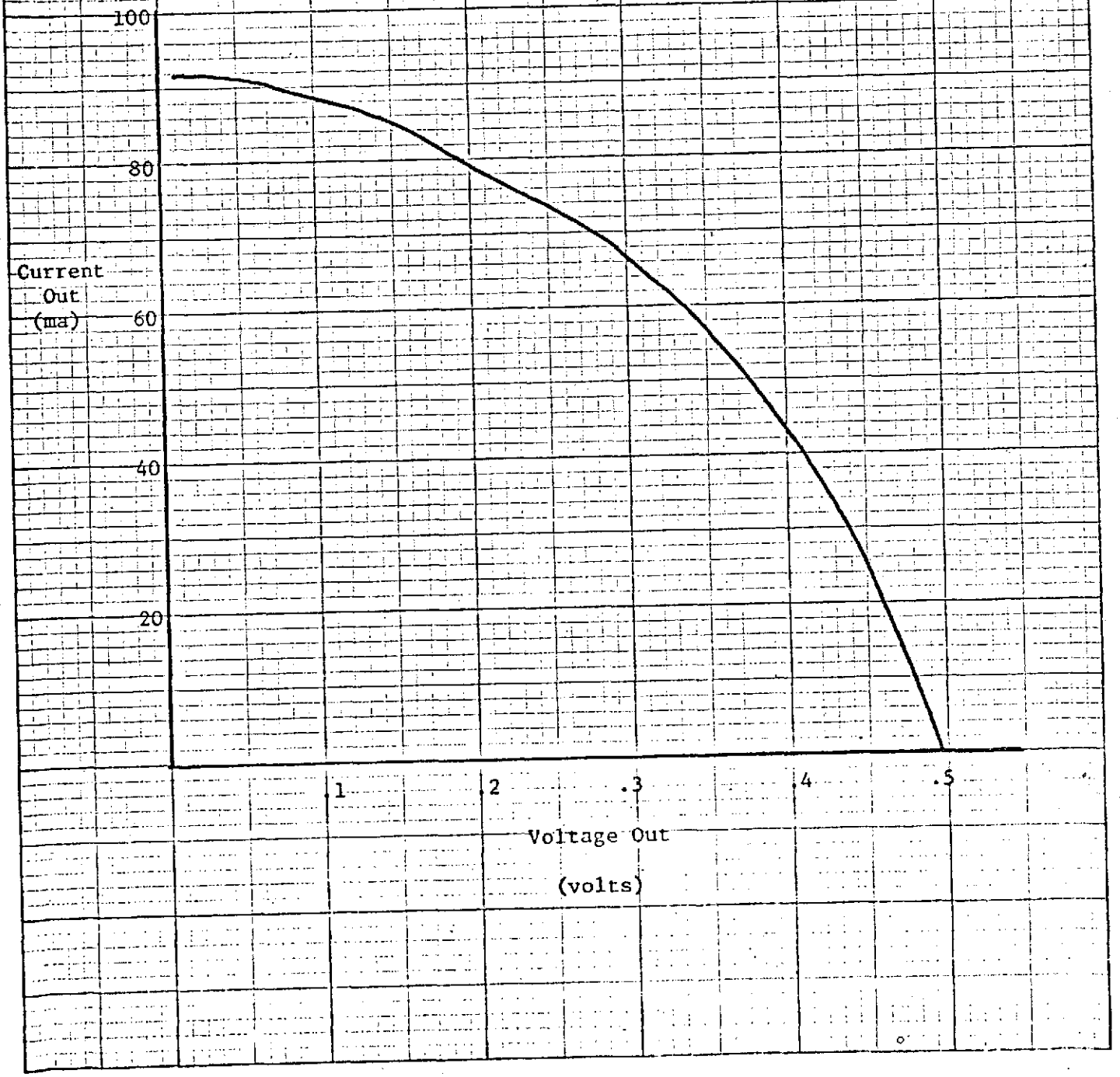
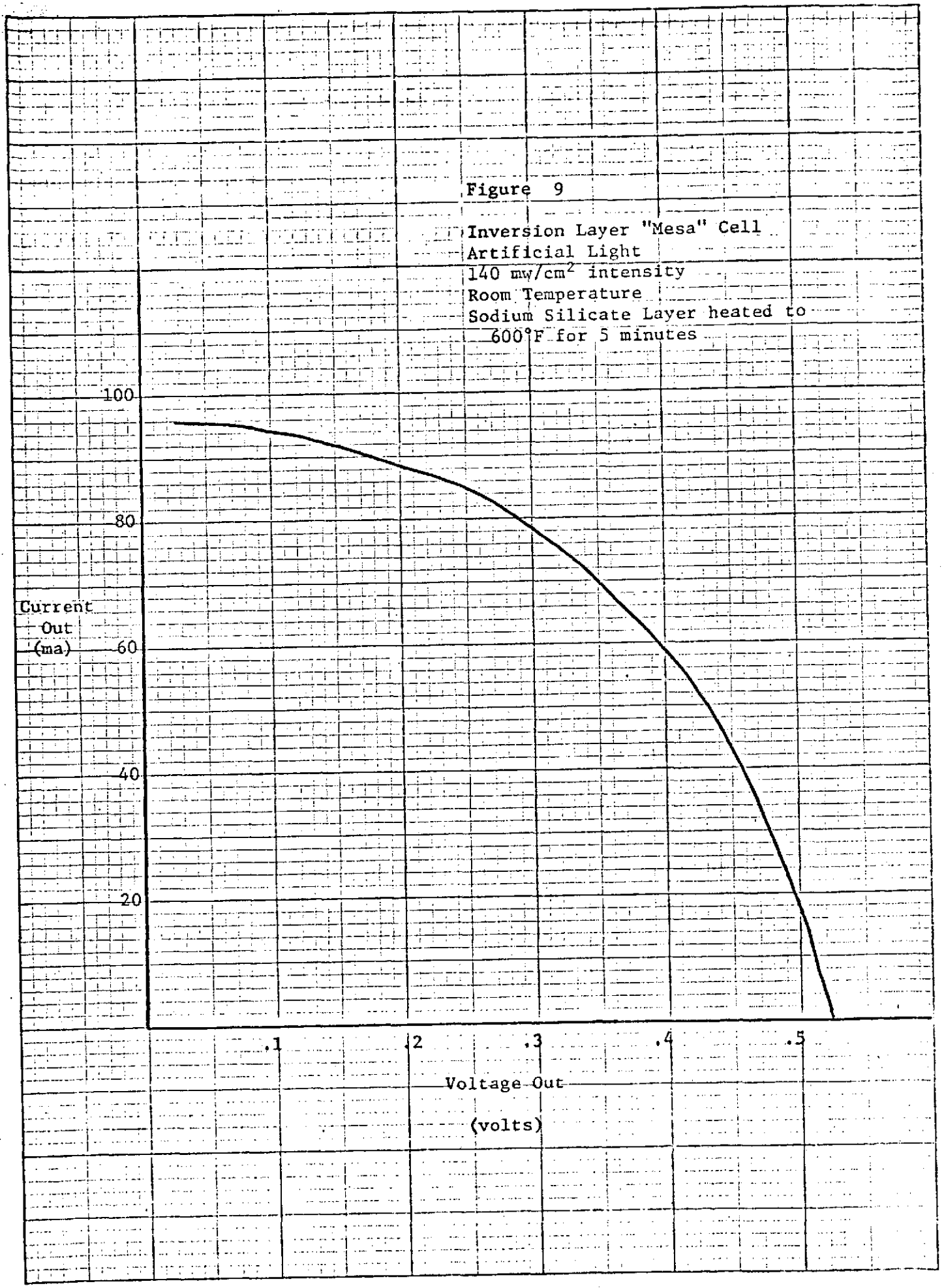


Figure 8

Inversion Layer "Mesa" Cell
Artificial Light
140 mw/cm^2 intensity
Room Temperature
Sodium Silicate Layer heated to
400°F for 5 minutes





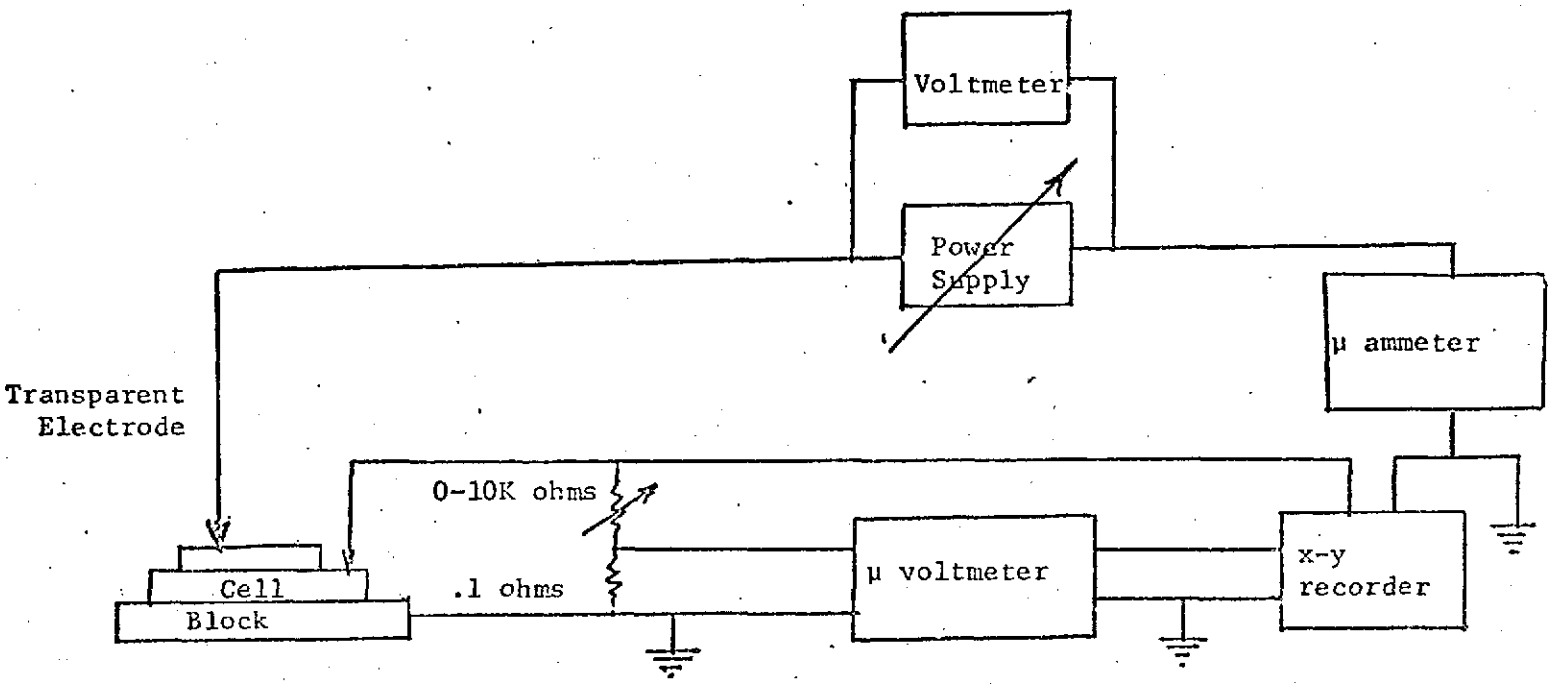


Fig. 10 Block Diagram of I-V Plotter

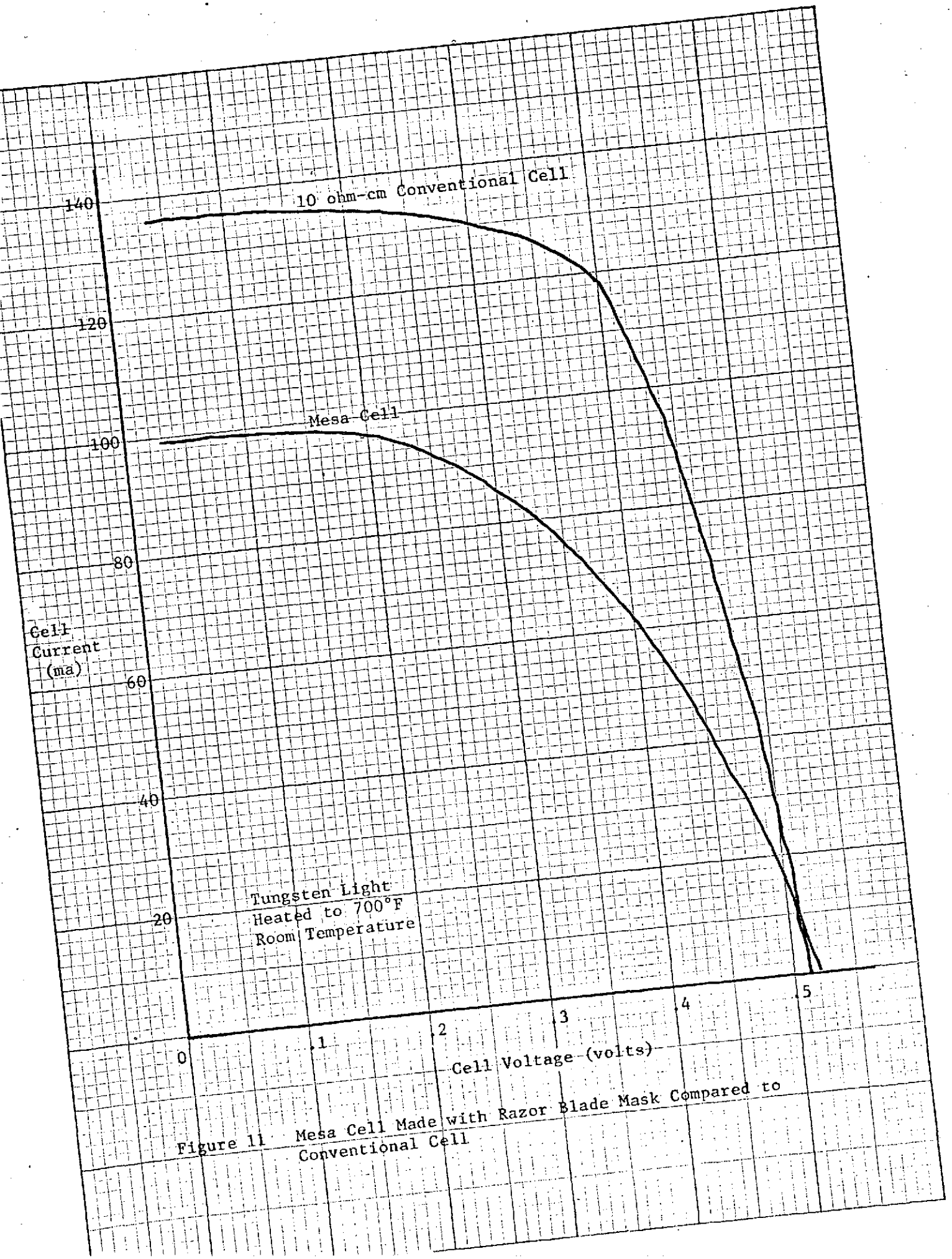


Figure 11 Mesa Cell Made with Razor Blade Mask Compared to Conventional Cell

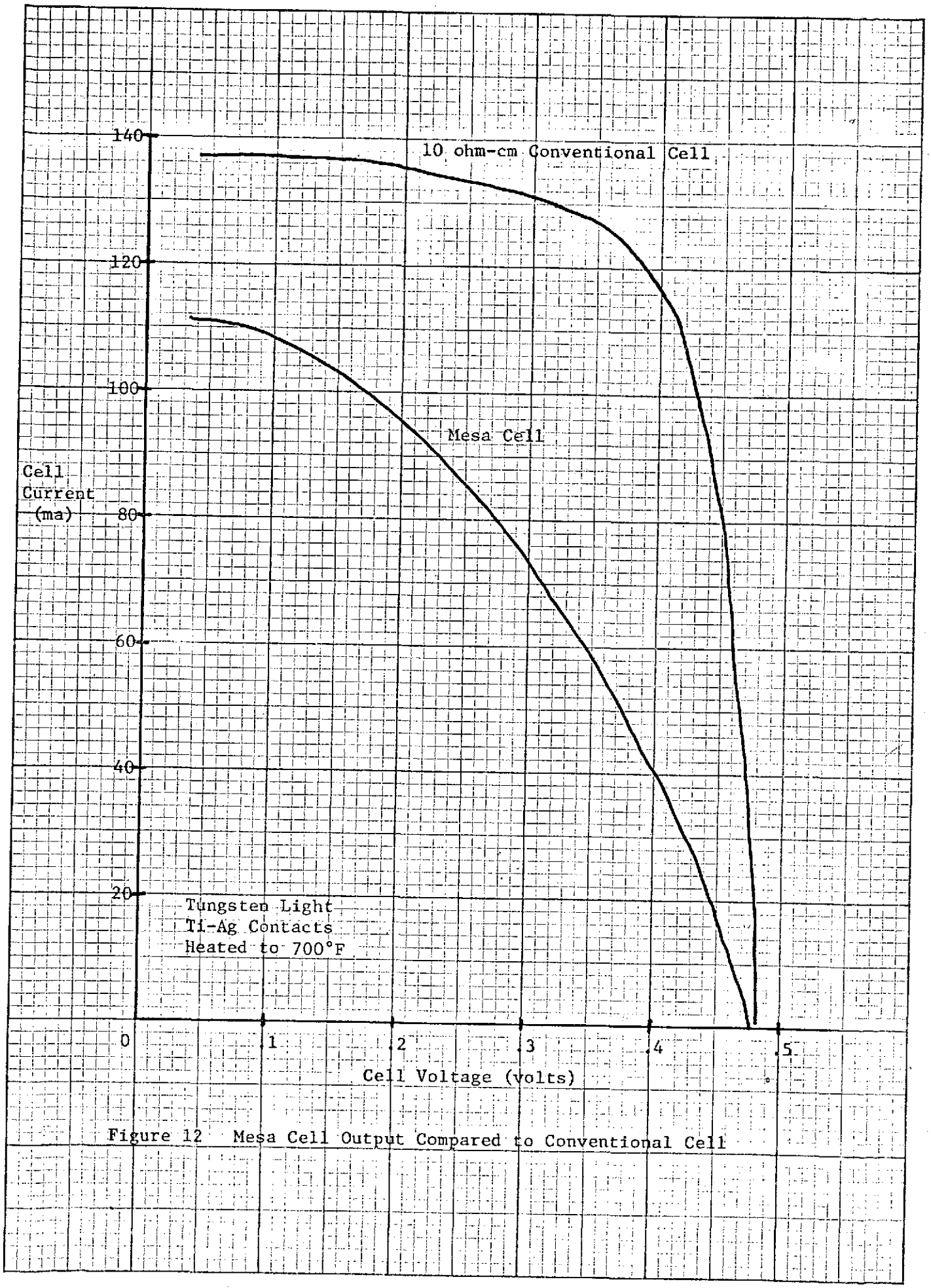


Figure 12 Mesa Cell Output Compared to Conventional Cell